FET

Refine Search

Search Results -

Terms	Documents
L7 and capacit$	1

Database:

US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L21

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Friday, May 26, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=PGPB; THES=ASSIGNEE; PLUR=YES; OP=OR		
L21	L7 and capacit$	1	L21
	DB=USPT; THES=ASSIGNEE; PLUR=YES; OP=OR		
L20	L18 and fet$	1	L20
L19	L18 and fet$	1	L19
L18	5261694.pn.	1	L18
L17	US-5666065-A.did.	1	L17

	DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; THES=ASSIGNEE; PLUR=YES; OP=OR		
L16	L15 and FET$	7	L16
L15	restraint$ and (vehicle or automobile or car or flight or airplane) and (fir$ near2 circuit)	46	L15
	DB=USPT; THES=ASSIGNEE; PLUR=YES; OP=OR		
L14	5430314.pn.	1	L14
	DB=PGPB; THES=ASSIGNEE; PLUR=YES; OP=OR		
L13	l7 and restraint$	1	L13
L12	20020121810	1	L12
	DB=USPT; THES=ASSIGNEE; PLUR=YES; OP=OR		
L11	20020121810	0	L11
L10	6878996.pn.	1	L10
	DB=PGPB; THES=ASSIGNEE; PLUR=YES; OP=OR		
L9	L7 and 11	1	L9
L8	L7 and supply$	1	L8
L7	20040108698	1	L7
	DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; THES=ASSIGNEE; PLUR=YES; OP=OR		
L6	L5 and (vehicle or automobile or car or flight or airplane)	0	L6
L5	L4 and @ad<=20021126	4	L5
L4	l2 or L3	10	L4
L3	"reverse diode" and "N-channel FET"	6	L3
L2	"reverse diode" and "N-type FET"	4	L2
	DB=USPT; THES=ASSIGNEE; PLUR=YES; OP=OR		
L1	6142130.pn.	1	L1

END OF SEARCH HISTORY

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L16: Entry 7 of 7 File: DWPI Dec 16, 1992

DERWENT-ACC-NO: 1992-417372
DERWENT-WEEK: 199952

TITLE: Vehicle passenger restraint firing circuit - uses microprocessor to control operation with diagnostic ASIC monitoring crash sensor to bias safer sensor and replace inoperable FET under failure conditions

INVENTOR: MUSSER, K E; PAYE, J R ; WHITE, C W

PATENT-ASSIGNEE: AUTOMOTIVE SYSTEMS LAB INC (AUTON)

PRIORITY-DATA: 1991US-0715344 (June 14, 1991)

Search Selected Search ALL Clear

PATENT-FAMILY:

	PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
☐	EP 518501 A1	December 16, 1992	E	007	B60R021/00
☐	KR 126667 B1	December 26, 1997		000	B60R021/16
☐	AU 9218036 A	December 24, 1992		000	B60R021/32
☐	CA 2069214 A	December 15, 1992		000	B60R021/32
☐	US 5261694 A	November 16, 1993		006	B60R021/16
☐	EP 518501 B1	March 20, 1996	E	009	B60R021/00
☐	DE 69209151 E	April 25, 1996		000	B60R021/00
☐	CA 2069214 C	December 17, 1996		000	B60R021/32

DESIGNATED-STATES: DE ES FR GB IT DE ES FR GB IT

CITED-DOCUMENTS:1.Jnl.Ref; EP 305656 ; US 4958851 ; US 5083276 ; US 5085464 ; 01Jnl.Ref

APPLICATION-DATA:

PUB-NO	APPL-DATE	APPL-NO	DESCRIPTOR
EP 518501A1	May 19, 1992	1992EP-0304499	
KR 126667B1	June 12, 1992	1992KR-0010227	
AU 9218036A	June 5, 1992	1992AU-0018036	
CA 2069214A	May 22, 1992	1992CA-2069214	
US 5261694A	June 14, 1991	1991US-0715344	

EP 518501B1	May 19, 1992	1992EP-0304499	
DE 69209151E	May 19, 1992	1992DE-0609151	
DE 69209151E	May 19, 1992	1992EP-0304499	
DE 69209151E		EP 518501	Based on ... ..
CA 2069214C	May 22, 1992	1992CA-2069214	

INT-CL (IPC): B60R 21/00; B60R 21/16; B60R 21/32

ABSTRACTED-PUB-NO: EP 518501A
BASIC-ABSTRACT:

The circuit has a relatively-low-threshold acceleration-responsive switch (14) of an acceleration sensor (safing sensor) (16) in series with parallel firing legs (18a,18b) each having in series an explosive squib (20) and a FET (22), all operating under the control of a microprocessor (24) which responds to the output from an electronic crash sensor (16).

A Diagnostic ASIC (44) under the control of the microprocessor monitors the performance of the crash sensor and on detection of a failure applies a current to the safer integral test coil (38) to bias the switch contacts away from operation. The microprocessor the turns on another FET (46) to pull down to ground one side of the squib to replace the inoperable FET.

ADVANTAGE - Provides circuit with two sensors in series for improved reliability and includes maintaining operation under single sensor failure conditions.

ABSTRACTED-PUB-NO: EP 518501B
EQUIVALENT-ABSTRACTS:

A control circuit for actuating a safety restraint in a motor vehicle comprising: a firing path (12,18) having in series a first normally-open switch means (14,16) for closing in response to vehicle therefore, a current-responsive trigger means (20) for actuating said safety restraint, and a second normally-open switch means (22) for closing in response to a second threshold value higher than said first threshold value; means (28) for applying a voltage across said firing path; failure detecting means (44) for detecting a failure of said first switch means (14,16) and/or said second switch means (22); threshold-adjusting means (36,38) responsive to said failure detecting means (44) for increasing the threshold value of said first switch means (14,16), wherein said threshold-adjusting means (36,38) operates to increase the threshold value of said first switch means (14,16) upon detection of a failure of said second switch means (22); shunt means (46), responsive to said failure detecting means (44) and operation of said threshold-adjusting means (36,38), for shunting said second switch means (22), wherein said shunt means (46) operates to shunt said second switch means (22) after operation of said threshold-adjusting means (36,38) upon a detection of a failure of said second switch means (22); characterised in that said control circuit further comprises: sensor means (26) for generating a first signal representative of instantaneous vehicle acceleration; processor means (24) responsive to said first signal for generating a second signal when said first signal indicates a condition corresponding to the second threshold value requiring actuation of said safety restraint; and wherein said second switch means is in communication with said processor means (24) and, in use, closes in response to generation of said second signal; said failure detecting means (44) is additionally for detecting a failure of said sensor means (26) and/or said processor means (24); said shunt means (46) is additionally for shunting said second switch means (22) upon detection of a failure of said sensor means (26) and/or said processor means (24); and said threshold adjusting means (36,38) also operates to increase the threshold value of said first switch means (14,16) upon

detection of a failure of said sensor means (26) and/or processor means (24) and wherein operation of said threshold-adjusting means (36,38) is, in use, inhibited upon detection of a failure of said first switch means (14,16).

US 5261694A

The control circuit for a vehicle passenger restraint includes a firing path including in series: a first, normally-open, acceleration-responsive switch which closes in response to an acceleration input exceeding a first threshold, the first switch being shunted by a first shunting resistor. A trigger actuates the restraint. The trigger having internal electrical resistance less than the resistance of the first shunting resistor. Second and third normally-open, electrically-operated switches are provided. The second switch is shunted by a second shunting resistor having a resistance greater than the internal resistance of the trigger. A device applies a voltage across the firing path. An electronic sensor detects an acceleration exceeding a second threshold, which is nominally greater than the first threshold.

A microprocessor responds to the electronic sensor for operating the controlling the second switch. The microprocessor closes the second switch when the electronic sensor senses an acceleration exceeding the second threshold. A failure-detector senses a failure of first switch, the electronic sensor, the microprocessor, or the second switch. A first device responds to the failure-detector for increasingly biasing the first switch in the normally-open position. A second device responds to the failure-detector by operating the third switch.

USE/ADVANTAGE - for vehicle passenger restraint e.g. air bags. Continuing circuit viability notwithstanding single point failure.

CHOSEN-DRAWING: Dwg.1/1 Dwg.1/1 Dwg.1/1

DERWENT-CLASS: Q17 S02 T01 X22
EPI-CODES: S02-G03; T01-J07C; X22-J07;

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Hit List

First Hit Your wildcard search against 10000 terms has yielded the results below.

Your result set for the last L# is incomplete.

The probable cause is use of unlimited truncation. Revise your search strategy to use limited truncation.

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Search Results - Record(s) 1 through 7 of 7 returned.

☐ 1. Document ID: US 5668723 A

Using default format because multiple data bases are involved.

L16: Entry 1 of 7 File: USPT Sep 16, 1997

US-PAT-NO: 5668723
DOCUMENT-IDENTIFIER: US 5668723 A

TITLE: Method and apparatus for sensing a vehicle crash using crash energy

DATE-ISSUED: September 16, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Blackburn; Brian K.	Rochester	MI		

US-CL-CURRENT: 701/45

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 2. Document ID: US 5216607 A

L16: Entry 2 of 7 File: USPT Jun 1, 1993

US-PAT-NO: 5216607
DOCUMENT-IDENTIFIER: US 5216607 A
**** See image for Certificate of Correction ****

TITLE: Method and apparatus for sensing a vehicle crash using energy and velocity as measures of crash violence

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 3. Document ID: US 4990884 A

L16: Entry 3 of 7 File: USPT Feb 5, 1991

US-PAT-NO: 4990884
DOCUMENT-IDENTIFIER: US 4990884 A

TITLE: Method and apparatus for testing an airbag restraint system

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 4. Document ID: US 4835513 A

L16: Entry 4 of 7 File: USPT May 30, 1989

US-PAT-NO: 4835513
DOCUMENT-IDENTIFIER: US 4835513 A
**** See image for Certificate of Correction ****

TITLE: Method and apparatus for testing an airbag restraint system

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 5. Document ID: US 5872460 A

L16: Entry 5 of 7 File: DWPI Feb 16, 1999

DERWENT-ACC-NO: 1999-166796
DERWENT-WEEK: 199914

TITLE: FET based firing circuit test apparatus in supplemental inflatable restraint (SIR) system

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 6. Document ID: US 5666065 A

L16: Entry 6 of 7 File: DWPI Sep 9, 1997

DERWENT-ACC-NO: 1997-456916
DERWENT-WEEK: 199742

TITLE: Test circuit for FETs of firing circuit of inflatable restraint system of vehicle - biasses squib to intermediate voltage and turns on each FET alone to apply battery or ground voltage to squib, and high and low voltage detectors sense voltage excursion past respective thresholds to verify FET operation

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KMC | Draw D

□ 7. Document ID: EP 518501 A1, KR 126667 B1, AU 9218036 A, CA 2069214 A, US 5261694 A, EP 518501 B1, DE 69209151 E, CA 2069214 C

L16: Entry 7 of 7 File: DWPI Dec 16, 1992

DERWENT-ACC-NO: 1992-417372
DERWENT-WEEK: 199952

TITLE: Vehicle passenger restraint firing circuit - uses microprocessor to control operation with diagnostic ASIC monitoring crash sensor to bias safer sensor and replace inoperable FET under failure conditions

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KMC | Draw D

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
L15 and FET$	7

Display Format: [-] Change Format

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L18: Entry 1 of 1 File: USPT Nov 16, 1993

US-PAT-NO: 5261694
DOCUMENT-IDENTIFIER: US 5261694 A
**** See image for Certificate of Correction ****

TITLE: Reconfigurable air bag firing circuit

DATE-ISSUED: November 16, 1993

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
White; Craig W.	Grosse Pointe	MI		
Musser; Kevin E.	Farmington	MI		
Paye; James R.	Roseville	MI		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Automotive Systems Laboratory, Inc.	Farmington Hills	MI			02

APPL-NO: 07/715344 [PALM]
DATE FILED: June 14, 1991

INT-CL-ISSUED: [05] B60R 21/16

US-CL-ISSUED: 280/735; 307/10.1
US-CL-CURRENT: 280/735; 307/10.1

FIELD-OF-CLASSIFICATION-SEARCH: 280/735, 180/274, 180/282, 307/10.1, 340/436, 340/438
See application file for complete search history.

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
4851705	July 1989	Musser et al.	280/735
4958851	September 1990	Behr et al.	280/735
5060504	October 1991	White	73/1D

☐ 5085464 February 1992 Behr et al. 340/436

ART-UNIT: 316

PRIMARY-EXAMINER: Tyson; Karin L.

ATTY-AGENT-FIRM: Lyon & Delevie

ABSTRACT:

An air bag firing circuit comprises a firing path which includes in series a safing sensor, a squib, and a FET operated under microprocessor control in response to the output of an electronic crash sensor. A power supply maintains a known voltage across the firing path sufficient to explode the squib upon simultaneous "closure" of both the safing sensor and the FET operated by the microprocessor in response to crash sensor output. Normally, upon detection of a failure in the electronic crash sensor, its supporting electronics, or the FET actuated in response thereto, the microprocessor reconfigures the firing threshold of the safing sensor, as by applying a current to its integral test coil to increasingly bias the sensor's inertial mass away from its switch contacts. However, if a failure of the safing sensor is detected, reconfiguration of its threshold is inhibited notwithstanding the failure of other circuit components to prevent inadvertent deployment of the air bag. Once the safing sensor is reconfigured, the microprocessor turns on another FET to pull one side of the squib to ground, thereby removing the inoperable FET from the firing path and ensuring continued protection of the vehicle passengers until the sensor is serviced or replaced.

5 Claims, 1 Drawing figures

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L20: Entry 1 of 1 File: USPT Nov 16, 1993

DOCUMENT-IDENTIFIER: US 5261694 A
**** See image for Certificate of Correction ****
TITLE: Reconfigurable air bag firing circuit

Abstract Text (1):
An air bag firing circuit comprises a firing path which includes in series a safing sensor, a squib, and a FET operated under microprocessor control in response to the output of an electronic crash sensor. A power supply maintains a known voltage across the firing path sufficient to explode the squib upon simultaneous "closure" of both the safing sensor and the FET operated by the microprocessor in response to crash sensor output. Normally, upon detection of a failure in the electronic crash sensor, its supporting electronics, or the FET actuated in response thereto, the microprocessor reconfigures the firing threshold of the safing sensor, as by applying a current to its integral test coil to increasingly bias the sensor's inertial mass away from its switch contacts. However, if a failure of the safing sensor is detected, reconfiguration of its threshold is inhibited notwithstanding the failure of other circuit components to prevent inadvertent deployment of the air bag. Once the safing sensor is reconfigured, the microprocessor turns on another FET to pull one side of the squib to ground, thereby removing the inoperable FET from the firing path and ensuring continued protection of the vehicle passengers until the sensor is serviced or replaced.

Brief Summary Text (10):
The improved control circuit for a vehicle passenger safety restraint of the instant invention comprises a low-threshold acceleration sensor, or "safing sensor," whose acceleration-responsive switch is connected in series with an explosive squib and a FET, with the FET closing under microprocessor control in response to the output of an electronic sensor employing a relatively-higher threshold. Upon the detection of a failure of the crash-discriminating electronic acceleration sensor and/or its supporting electronics, and after confirmation of continuing safing sensor functionality, the circuit reconfigures the firing circuit by raising the acceleration threshold of the safing sensor and then, after a suitable delay, removing the FET from the firing path by pulling down the side of the squib opposite the safing sensor to ground. In the preferred embodiment of the invention, the safing sensor is tested, and its threshold alternatively raised, by passing a current from a constant current source through a test coil integral to the sensor, as controlled by an application specific integrated circuit.

Detailed Description Text (2):
Referring to the drawing, an exemplary air bag firing circuit 10 according to the instant invention comprises a firing path 12 which includes, in series, the normally-open, relatively-low-threshold acceleration-responsive switch 14 of an acceleration sensor (hereinafter "safing sensor 16"); and parallel firing path legs 18a and 18b each having in series an explosive squib 20 for triggering deployment of a driver's-side and a passenger's-side air bag, respectively (both not shown), and a FET ("firing FET 22") for pulling down the side of each squib 20 opposite the safing sensor 16 to ground when operated by a microprocessor 24. The microprocessor

24 is itself responsive to the output of an electronic crash sensor integrated within an Application Specific Integrated Circuit ("Sensor ASIC 26"), as more fully described below.

Detailed Description Text (3):
A power supply 28 applies a known supply voltage V.sub.s across the firing path 12 sufficient to explode each squib 20 upon the simultaneous closure of the safing sensor's switch 14 and the firing FET 22 connected to the squib 20. The power supply 28 includes a capacitor 30 and charge pump 32 to maintain the applied voltage V.sub.s if the battery 34 connected thereto malfunctions or is otherwise isolated therefrom during a vehicle collision.

Detailed Description Text (5):
Similarly, a constructed embodiment of the crash sensor integrated into the Sensor ASIC 26 is disclosed in our co-pending U.S. patent application Ser. No. 07/413,318 filed Sep. 27, 1989, now U.S. Pat. No. 5,060,504 issued Oct. 29, 1991, and entitled "Self-Calibrating Accelerometer," which teaching is also hereby incorporated herein by reference. Simply stated, the electronic sensor within the Sensor ASIC 26 provides an analog output proportional to vehicle acceleration, as through the incorporation of a piezoresistive element in the support beam of the sensor's micromachined cantilevered inertial mass. After analog-to-digital conversion of the electronic sensor's output within the Sensor ASIC 26, the resulting acceleration data is communicated to the microprocessor 24 via a Serial Peripheral Interface ("SPI 40"), whereupon the microprocessor 24 determines whether a threshold acceleration has been exceeded, thereby indicating a crash condition. If a crash condition is indicated, the microprocessor 24 turns on the firing FETs 22 to pull down the side of each squib 20 opposite the safing sensor 16 to ground.

Detailed Description Text (6):
The normally-open switch 14 of the safing sensor 16 and each firing FET 22 are shunted by a resistor 42 of like nominal resistance. Preferably, the nominal resistance of the shunting resistors 42 is several orders of magnitude larger than the nominal internal resistance of each of the squibs 20. In normal operation, the shunting resistors 42 maintain a relatively-low current flow through the firing path 12 and, hence, through the squibs 20 thereof. Upon the simultaneous closure of the safing sensor 16 and the firing FETs 22 in response to an acceleration exceeding the respective thresholds of the safing sensor 16 and the electronic crash sensor within the ASIC 26 (as determined by the microprocessor 24), the shunting resistors 42 are shorted and the current flowing through each squib 20 increases to a value above the firing threshold thereof to explode same and trigger deployment of each air bag.

Detailed Description Text (8):
An additional FET ("reconfiguration FET 46") is connected to the firing path 12 at points on each leg 18a and 18b between the squib 20 and the firing FET 22 thereon via a diode 48, with the reconfiguration FET 46 being controlled by the Sensor ASIC 26. The reconfiguration FET 46 allows the Sensor ASIC 26 to pull the side of each squib 20 opposite the safing sensor 16 to ground when the Diagnostic ASIC 44 detects a failure of the Sensor ASIC's integral electronic crash sensor or its supporting electronics, including failures of the microprocessor 24 or the FETs 22 controlled by the microprocessor 24.

Detailed Description Text (9):
Under the instant invention, reconfiguration of the circuit's firing path 12 is controlled by the two ASICs 26 and 44, the constant current source 36, and the microprocessor 24, as follows: in the circuit's normal mode of operation, the microprocessor 24 initiates firing-path reconfiguration through the use of a watchdog timer in the Diagnostic ASIC 44. Specifically, the microprocessor 24 periodically resets the timer by sending reconfiguration pulses 50 to the Diagnostic ASIC 44. If the microprocessor 24 detects a failure of the Sensor ASIC

26, e.g., the failure of its electronic crash sensor to properly respond to acceleration, or excessive electromagnetic interference ("EMI"), the microprocessor 24 stops transmitting reconfiguration pulses 50 to the Diagnostic ASIC 44, and the timer runs out to trigger reconfiguration. Similarly, the microprocessor 24 will request reconfiguration of the circuit's firing path 12 upon detecting a failure of any of the firing FETs 22 or the reconfiguration FET 46. A suitable period for the watchdog timer is believed to be about 250 msec.

Detailed Description Text (12):
Once triggered, the reconfiguration sequence for the instant circuit 10 is as follows: the Diagnostic ASIC 44 first determines whether the safing sensor 16 has been shorted to ground by monitoring the voltage at a point 58 on the firing path 12 between the safing sensor 16 and both squibs 20. If continuing safing sensor functionality (and firing path integrity) is confirmed, the Diagnostic ASIC 44 will send signals 62, 64, and 66 through PHASE, I.sub.0 and I.sub.1 terminals of the constant current source 36, respectively, whereby the current 60 is directed in a second direction through the sensor's test coil 38 to increase its threshold by increasingly biasing its switch 14 in the open position. When the current source 36 is turned on, the current source 36 also generates current sense pulses 68 which are counted by the Sensor ASIC 26. After a suitable number of pulses 68 are counted by the Sensor ASIC 26, thereby representing a reasonable time delay to permit the reconfigured safing sensor 16 to achieve a steady-state heightened threshold, the Sensor ASIC 26 turns on the reconfiguration FET 46 to pull down the sides of the squibs 20 opposite the safing sensor 16 to ground. The firing path 12 of the instant circuit 10 is thus reconfigured, with the heightened-threshold safing sensor 16 thereafter operating as the circuit's crash-discriminating sensor.

Detailed Description Text (14):
If the monitored voltage at point 58 on the firing path 12 indicates a shorted safing sensor 16, the Diagnostic ASIC 44 terminates the reconfiguration sequence, since it otherwise might result in inadvertent deployment of the air bags if the reconfiguration FET 46 would thereafter be turned on.

Detailed Description Text (16):
While the preferred embodiment of the invention has been disclosed, it should be appreciated that the invention is susceptible of modification without departing from the spirit of the invention or the scope of the subjoined claims. For example, under the instant invention, the Sensor and Diagnostic ASICs 26 and 44 may be repackaged so as to place all reconfiguration control in a separate Reconfiguration ASIC which is therefore wholly independent from the components providing diagnostic capability. Such a reconfiguration ASIC would preferably incorporate V.sub.s, current sense, and voltage monitoring inputs; PHASE, I.sub.0, I.sub.1, reconfiguration FET control, and reconfiguration pulse outputs; and SPI communication with other circuit components regarding electronic sensor output, test signal requests, and other circuit component status communication.

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FET

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Search Results - Record(s) 1 through 7 of 7 returned.

☐ 1. Document ID: US 5668723 A

Using default format because multiple data bases are involved.

L16: Entry 1 of 7 File: USPT Sep 16, 1997

US-PAT-NO: 5668723
DOCUMENT-IDENTIFIER: US 5668723 A

TITLE: Method and apparatus for sensing a vehicle crash using crash energy

DATE-ISSUED: September 16, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Blackburn; Brian K.	Rochester	MI		

US-CL-CURRENT: 701/45

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw. D

☐ 2. Document ID: US 5216607 A

L16: Entry 2 of 7 File: USPT Jun 1, 1993

US-PAT-NO: 5216607
DOCUMENT-IDENTIFIER: US 5216607 A
**** See image for Certificate of Correction ****

TITLE: Method and apparatus for sensing a vehicle crash using energy and velocity as measures of crash violence

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw. D

☐ 3. Document ID: US 4990884 A

L16: Entry 3 of 7   File: USPT   Feb 5, 1991

US-PAT-NO: 4990884
DOCUMENT-IDENTIFIER: US 4990884 A

TITLE: Method and apparatus for testing an airbag restraint system

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 4. Document ID: US 4835513 A

L16: Entry 4 of 7   File: USPT   May 30, 1989

US-PAT-NO: 4835513
DOCUMENT-IDENTIFIER: US 4835513 A
**** See image for Certificate of Correction ****

TITLE: Method and apparatus for testing an airbag restraint system

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 5. Document ID: US 5872460 A

L16: Entry 5 of 7   File: DWPI   Feb 16, 1999

DERWENT-ACC-NO: 1999-166796
DERWENT-WEEK: 199914

TITLE: FET based firing circuit test apparatus in supplemental inflatable restraint (SIR) system

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 6. Document ID: US 5666065 A

L16: Entry 6 of 7   File: DWPI   Sep 9, 1997

DERWENT-ACC-NO: 1997-456916
DERWENT-WEEK: 199742

TITLE: Test circuit for FETs of firing circuit of inflatable restraint system of vehicle - biasses squib to intermediate voltage and turns on each FET alone to apply battery or ground voltage to squib, and high and low voltage detectors sense voltage excursion past respective thresholds to verify FET operation

☐ 7. Document ID: EP 518501 A1, KR 126667 B1, AU 9218036 A, CA 2069214 A, US 5261694 A, EP 518501 B1, DE 69209151 E, CA 2069214 C

L16: Entry 7 of 7 File: DWPI Dec 16, 1992

DERWENT-ACC-NO: 1992-417372
DERWENT-WEEK: 199952

TITLE: Vehicle passenger restraint firing circuit - uses microprocessor to control operation with diagnostic ASIC monitoring crash sensor to bias safer sensor and replace inoperable FET under failure conditions

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

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Terms	Documents
L15 and FET$	7

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L16: Entry 1 of 7 File: USPT Sep 16, 1997

US-PAT-NO: 5668723
DOCUMENT-IDENTIFIER: US 5668723 A

TITLE: Method and apparatus for sensing a vehicle crash using crash energy

DATE-ISSUED: September 16, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Blackburn; Brian K.	Rochester	MI		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
TRW Vehicle Safety Systems Inc.	Lyndhurst	OH			02

APPL-NO: 08/650424 [PALM]
DATE FILED: May 20, 1996

PARENT-CASE:
RELATED APPLICATIONS This application is a continuation-in-part of U.S. patent application Ser. No. 07/818,280, filed Jan. 8, 1992, now U.S. Pat. No. 5,546,307 entitled "METHOD AND APPARATUS FOR DISCRIMINATING VEHICLE CRASH CONDITIONS" filed in the name of Joseph F. Mazur et al. which is a continuation-in-part of U.S. Ser. No. 07/520,417, filed May 11, 1990, in the name of Diller et al., entitled METHOD AND APPARATUS FOR SENSING A VEHICLE CRASH USING ENERGY AND VELOCITY AS MEASURES OF CRASH VIOLENCE" which is now U.S. Pat. No. 5,216,607, issued Jun. 1, 1993, which is a continuation-in-part of U.S. Ser. No. 07/358,875, filed May 30, 1989, in the name of Brian K. Blackburn entitled "METHOD AND APPARATUS FOR SENSING A VEHICLE CRASH", which is now U.S. Pat. No. 4,979,763 issued Dec. 25, 1990.

INT-CL-ISSUED: [06] B60 R 21/32

US-CL-ISSUED: 701/45
US-CL-CURRENT: 701/45

FIELD-OF-CLASSIFICATION-SEARCH: 364/424.055, 364/424.056, 364/424.057, 180/282, 180/232, 180/271, 280/728, 280/734, 280/735, 340/438, 340/436, 307/9.1, 307/10.1
See application file for complete search history.

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3703300	November 1972	Gillund et al.	280/150AB
☐	3870894	March 1975	Brede et al.	307/9
☐	3911391	October 1975	Held et al.	340/52H
☐	4020453	April 1977	Spies et al.	340/52H
☐	4166641	September 1979	Okada et al.	280/735
☐	4638179	January 1987	Mattes et al.	307/105B
☐	4804859	February 1989	Swart	307/105B
☐	4842301	June 1989	Feldmaier	280/735
☐	4851705	July 1989	Musser et al.	307/10.1
☐	4873452	October 1989	Morota et al.	307/10.1

ART-UNIT: 234

PRIMARY-EXAMINER: Teska; Kevin J.

ASSISTANT-EXAMINER: Walder, Jr.; Stephen J.

ATTY-AGENT-FIRM: Tarolli, Sundheim, Covell, Tummino & Szabo

ABSTRACT:

A method and apparatus is disclosed for providing a passenger restraint actuation signal for use in an actuatable passenger restraint system in a vehicle is provided. A sensor provides a signal indicative of crash acceleration. A crash energy value is determined from the crash acceleration signal and is compared against an energy threshold value. If the determined crash energy value equals or exceeds the energy threshold value, a passenger restraint actuation signal is provided.

2 Claims, 13 Drawing figures

L16: Entry 5 of 7 File: DWPI Feb 16, 1999

DERWENT-ACC-NO: 1999-166796
DERWENT-WEEK: 199914

TITLE: FET based firing circuit test apparatus in supplemental inflatable restraint (SIR) system

INVENTOR: ANDERSON, T; BENNETT, P T ; CONSTABLE, R K ; GRAY, R C ; RAVAS, R J

PATENT-ASSIGNEE: DELCO ELECTRONICS CORP (DELCN)

PRIORITY-DATA: 1996US-0726897 (October 4, 1996)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 5872460 A	February 16, 1999		011	G01R031/26

APPLICATION-DATA:

PUB-NO	APPL-DATE	APPL-NO	DESCRIPTOR
US 5872460A	October 4, 1996	1996US-0726897	

INT-CL (IPC): B60 R 21/32; G01 R 31/26

ABSTRACTED-PUB-NO: US 5872460A
BASIC-ABSTRACT:

NOVELTY - The gate drive circuits (26,28) are connected with logic module (42) that responds to detection results of current detectors (32,50) and voltage detectors (38,40). When the short condition is indicated by the detection result of the current detector, the selected FET is turned OFF, independent of the microprocessor based deployment controller (12).

DETAILED DESCRIPTION - The gate drive circuits (26,28) turn on a selected FET to test operability of such FET, in response from a microprocessor based deployment controller. The current detector detects firing circuit current and if this detection results exceeds current threshold, short condition is indicated. The voltage detectors are also connected to the firing circuit for detecting whether variance of voltage on squib between FETs serially coupled between voltage source and ground, exceeds set voltage threshold values where the threshold values are above and below a regulated voltage applied to the squib. When the detection result of the voltage detector indicates that detected voltage on squib breaches one of the voltage threshold values, then the selected FET is disabled.

USE - For supplemental inflatable restraint system for inflating airbag in

automotive vehicles.

ADVANTAGE - Facilitates rapid testing of FETs of SIR firing circuit even when it is subjected to wide ranges of voltages due to shorts. Even in case of resistive short, the short is detected by sensing abnormal loop voltage and thus turns off the selected FET. FETs of the SIR firing loop is tested without any danger of firing the squib even when short condition occurs.

DESCRIPTION OF DRAWING(S) - The figure depicts the SIR control for inflating airbag of automotive vehicle.

Microprocessor based deployment controller 12

Gate drive circuits 26,28

Current detectors 32,50

Voltage detectors 38,40

Logic module 42

ABSTRACTED-PUB-NO: US 5872460A
EQUIVALENT-ABSTRACTS:

CHOSEN-DRAWING: Dwg.1/5

DERWENT-CLASS: Q17 S01 S02 U11
EPI-CODES: S01-G02B; S02-J02E; U11-F01C5;

Previous Doc Next Doc Go to Doc#

L14: Entry 1 of 1 File: USPT Jul 4, 1995

US-PAT-NO: 5430314
DOCUMENT-IDENTIFIER: US 5430314 A

TITLE: Power device with buffered gate shield region

DATE-ISSUED: July 4, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Yilmaz; Hamza	Saratoga	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Siliconix Incorporated	Santa Clara	CA			02

APPL-NO: 07/873423 [PALM]
DATE FILED: April 23, 1992

INT-CL-ISSUED: [06] H01 L 29/10, H01 L 29/78, H01 L 27/14, H01 L 31/00

US-CL-ISSUED: 257/328; 257/294, 257/337, 257/340, 257/341
US-CL-CURRENT: 257/328; 257/294, 257/337, 257/340, 257/341, 257/E29.066, 257/E29.257

FIELD-OF-CLASSIFICATION-SEARCH: 357/23.4, 257/294, 257/328, 257/337, 257/340, 257/341
See application file for complete search history.

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4532534	July 1985	Ford et al.	357/23.4
☐	4631564	December 1986	Neilson et al.	357/23.4
☐	4819044	April 1989	Murakami	
☐	4985739	January 1991	Lapham et al.	357/22
☐	5136349	August 1992	Yilmaz et al.	357/23.4

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	CLASS
293846A1	May 1988	EP	
335750A3	April 1989	EP	
60-249367	December 1985	JP	
61-80860	April 1986	JP	
61-84865	April 1986	JP	
63-73564	April 1988	JP	
63-84070	April 1988	JP	
1-276770	November 1989	JP	
2-35780	February 1990	JP	
3173180	July 1991	JP	
2137811	October 1984	GB	
2166290	April 1986	GB	

OTHER PUBLICATIONS

Conference Record of the 1986 IEEE Industry Applications Society Annual Meeting, vol. 1, Oct. 1986, Denver, Colo., "Optimization of Power MOSFET Body Diode for Speed and Ruggedness", by Hamza Yilmaz et al., pp. 330-334.
"Design Optimization of Power MOSFET With Built-In Flyback Diode", by Yilmaz et al., Power Electronics Semiconductor Department, General Electric Co., Syracuse, N.Y., pp. 1-6.
"MOSPOWER Applications Handbook", Severns et al., Siliconix Incorporated, 1984, pp. 5-57 through 5-64.
"Semiconductor Power Devices", Sorab K. Ghandhi, Rensselaer Polytechnic Institute, John Wiley & Sons, N.Y., 1977, pp. 1-17 and 172-176.

ART-UNIT: 253

PRIMARY-EXAMINER: Crane; Sara W.

ASSISTANT-EXAMINER: Wallace; Valencia M.

ATTY-AGENT-FIRM: Skjerven, Morrill, MacPherson, Franklin & Friel

ABSTRACT:

The present invention provides a gate buffer region between a gate shield region and active cells of a power device. This gate buffer region may, for example, be a relatively narrow, strip-like doped region which extends into an epitaxial layer from an upper surface of the epitaxial layer. The gate shield region is connected to a source electrode of the power device via a relatively high impedance connection. The gate buffer region, on the other hand, is connected to the source electrode with a relatively low impedance connection. This relatively low impedance connection may, for example, be a substantially direct metallized connection from a metal source electrode to the gate buffer region at the surface of the epitaxial layer.

15 Claims, 18 Drawing figures

L16: Entry 6 of 7 File: DWPI Sep 9, 1997

DERWENT-ACC-NO: 1997-456916
DERWENT-WEEK: 199742

TITLE: Test circuit for FETs of firing circuit of inflatable restraint system of vehicle - biasses squib to intermediate voltage and turns on each FET alone to apply battery or ground voltage to squib, and high and low voltage detectors sense voltage excursion past respective thresholds to verify FET operation

INVENTOR: ANDERSON, T; CONSTABLE, R K ; RAVAS, R J

PATENT-ASSIGNEE: DELCO ELECTRONICS CORP (DELCN)

PRIORITY-DATA: 1996US-0651073 (May 22, 1996)

Search Selected Search ALL Clear

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 5666065 A	September 9, 1997		007	G01R031/28

APPLICATION-DATA:

PUB-NO	APPL-DATE	APPL-NO	DESCRIPTOR
US 5666065A	May 22, 1996	1996US-0651073	

INT-CL (IPC): B60 Q 1/00; G01 M 19/00; G01 R 31/28

ABSTRACTED-PUB-NO: US 5666065A
BASIC-ABSTRACT:

An automotive supplemental inflatable restraint system has a firing circuit containing a squib between two FETs serially coupled between a voltage source and ground for effecting inflation of a restraint, and a deployment circuit for controlling the firing circuit. The test circuit for FETs comprises a regulated voltage source applied to the squib. A

detector is coupled to the firing circuit for detecting variance of the voltage on the squib beyond set thresholds above and below the regulated voltage.

The gate responds to a test signal for turning on a selected FET so that the voltage on the squib varies beyond one of the thresholds while the selected FET is on. The gate has a logic circuit responsive to the detector for preventing conductance of the selected FET when the voltage breaches a threshold so that the selected FET, if turned on, is held on for only a short period. The logic circuit has a device for producing an output signal indicative of FET operability. If a short is present before the FET is commanded on, a detector and the logic circuit

prevents FET conduction to avoid firing or degrading the squib.

USE/ADVANTAGE - For rapidly testing FETs of SIR firing circuit while minimising likelihood of short occurring during testing. Also tests for shorts to battery or to ground with same circuit used for FET tests.

ABSTRACTED-PUB-NO: US 5666065A
EQUIVALENT-ABSTRACTS:

CHOSEN-DRAWING: Dwg.1/4

DERWENT-CLASS: Q16 S01 S02 T01 X22
EPI-CODES: S01-D01B5; S01-G04A1; S02-G03; S02-J02E; T01-J07C; X22-A07;

Previous Doc Next Doc Go to Doc#

Hit List

First Hit Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 1 of 1 returned.

☐ 1. Document ID: US 5666065 A

L17: Entry 1 of 1 File: USPT Sep 9, 1997

US-PAT-NO: 5666065
DOCUMENT-IDENTIFIER: US 5666065 A

TITLE: Fast acting FET test circuit for SIR diagnostics

DATE-ISSUED: September 9, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ravas; Richard Joseph	Kokomo	IN		
Anderson; Terrell	Carmel	IN		
Constable; Robert Keith	Kokomo	IN		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Delco Electronics Corp.	Kokomo	IN			02

APPL-NO: 08/651073 [PALM]
DATE FILED: May 22, 1996

INT-CL-ISSUED: [06] G01 R 31/28, B60 Q 1/00, G01 M 19/00

US-CL-ISSUED: 324/769; 324/505, 340/438
US-CL-CURRENT: 324/769; 324/505, 340/438

FIELD-OF-CLASSIFICATION-SEARCH: 324/769, 324/502, 324/505, 340/61, 340/436, 340/438, 280/735, 307/10.1
See application file for complete search history.

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
5081442	January 1992	Ito et al.	340/438
5166880	November 1992	Furvi	364/424.05

5268643 December 1993 Aso et al. 324/502

ART-UNIT: 223

PRIMARY-EXAMINER: Wieder; Kenneth A.

ASSISTANT-EXAMINER: Bowser; Barry C.

ATTY-AGENT-FIRM: Navarre; Mark A.

ABSTRACT:

The firing circuit of an inflatable restraint system is tested to verify operation of two FETs in series with a squib which are used to apply current to the squib. For the test the squib is biased to an intermediate voltage and each FET is turned on alone to apply battery or ground voltage to the squib. High and low voltage detectors sense the voltage excursion past respective thresholds to verify FET operation, and a logic circuit immediately turns off the FET to result in a very short FET on time. If a short is present before the FET is commanded on, a detector and the logic circuit prevents FET conduction to avoid firing or degrading the squib.

7 Claims, 4 Drawing figures

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
US-5666065-A.did.	1

Display Format: TI Change Format

10/729939

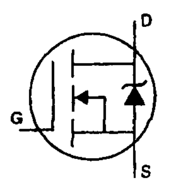
PD-9.868

International
IOR Rectifier

IRFL210

HEXFET® Power MOSFET

- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



V_{DSS} = 200V

$R_{DS(on)}$ = 1.5Ω

I_D = 0.96A

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-223 package is designed for surface-mounting using vapor phase, infra red, or wave soldering techniques. Its unique package design allows for easy automatic pick-and-place as with other SOT or SOIC packages but has the added advantage of improved thermal performance due to an enlarged tab for heatsinking. Power dissipation of greater than 1.25W is possible in a typical surface mount application.

SOT-223

DATA SHEETS

Absolute Maximum Ratings

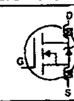
	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10 V	0.96	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10 V	0.60	
I_{DM}	Pulsed Drain Current ①	7.7	
P_D @ T_C = 25°C	Power Dissipation	3.1	W
P_D @ T_A = 25°C	Power Dissipation (PCB Mount)**	2.0	
	Linear Derating Factor	0.025	W/°C
	Linear Derating Factor (PCB Mount)**	0.017	
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	50	mJ
I_{AR}	Avalanche Current ①	0.96	A
E_{AR}	Repetitive Avalanche Energy ①	0.31	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

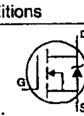
	Parameter	Min.	Typ.	Max.	Units
$R_{θJC}$	Junction-to-PCB	—	—	40	°C/W
$R_{θJA}$	Junction-to-Ambient (PCB mount)**	—	—	60	

** *When mounted on 1" square PCB (FR-4 or G-10 Material).*
For recommended footprint and soldering techniques refer to application note #AN-994.

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	—	—	V	V_{GS}=0V, I_D= 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.30	—	V/°C	Reference to 25°C, I_D= 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	1.5	Ω	V_{GS}=10V, I_D=0.58A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS}=V_{GS}, I_D= 250µA
g_{fs}	Forward Transconductance	0.51	—	—	S	V_{DS}=50V, I_D=0.58A ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS}=200V, V_{GS}=0V
		—	—	250		V_{DS}=160V, V_{GS}=0V, T_J=125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS}=20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS}=-20V
Q_g	Total Gate Charge	—	—	8.2	nC	I_D=3.3A
Q_{gs}	Gate-to-Source Charge	—	—	1.8		V_{DS}=160V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	4.5		V_{GS}=10V See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	8.2	—	ns	V_{DD}=100V
t_r	Rise Time	—	17	—		I_D=3.3A
$t_{d(off)}$	Turn-Off Delay Time	—	14	—		R_G=24Ω
t_f	Fall Time	—	8.9	—		R_D=30Ω See Figure 10 ④
L_D	Internal Drain Inductance	—	4.0	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	6.0	—		
C_{iss}	Input Capacitance	—	140	—	pF	V_{GS}=0V
C_{oss}	Output Capacitance	—	53	—		V_{DS}= 25V
C_{rss}	Reverse Transfer Capacitance	—	15	—		f=1.0MHz See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	0.96	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	7.7		
V_{SD}	Diode Forward Voltage	—	—	2.0	V	T_J=25°C, I_S=0.96A, V_{GS}=0V ④
t_{rr}	Reverse Recovery Time	—	150	310	ns	T_J=25°C, I_F=3.3A
Q_{rr}	Reverse Recovery Charge	—	0.60	1.4	µC	di/dt=100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is neglegible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

② V_{DD}=50V, starting T_J=25°C, L=81mH R_G=25Ω, I_{AS}=0.96A (See Figure 12)

③ I_{SD}≤3.3A, di/dt≤70A/µs, V_{DD}≤$V_{(BR)DSS}$, T_J≤150°C

④ Pulse width ≤ 300 µs; duty cycle ≤2%.

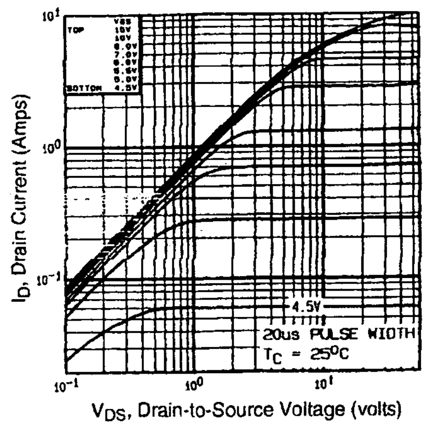


Fig 1. Typical Output Characteristics, T_C=25°C

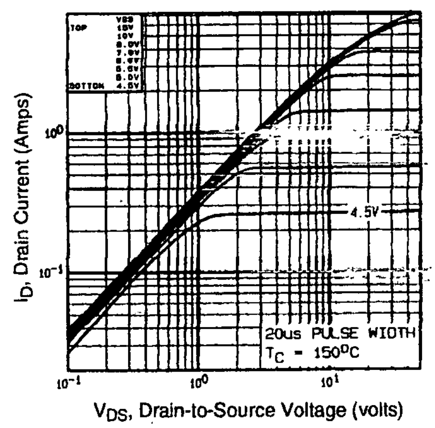


Fig 2. Typical Output Characteristics, T_C=150°C

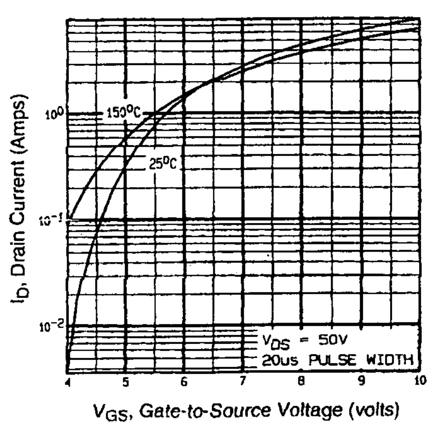


Fig 3. Typical Transfer Characteristics

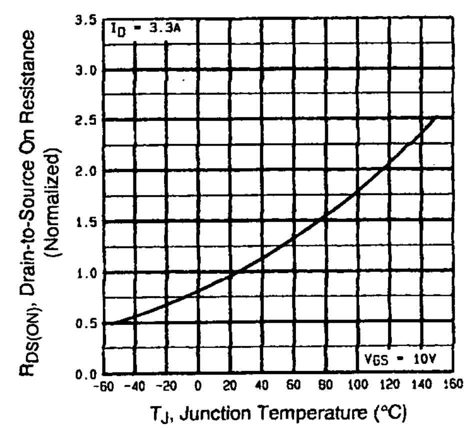


Fig 4. Normalized On-Resistance Vs. Temperature

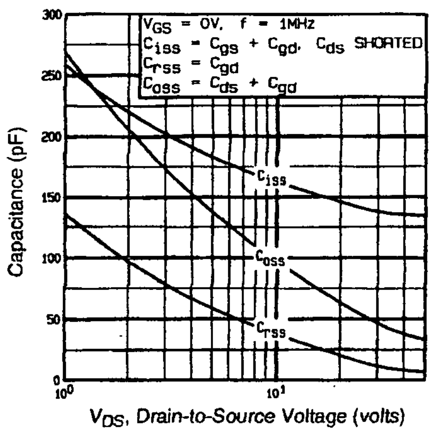


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

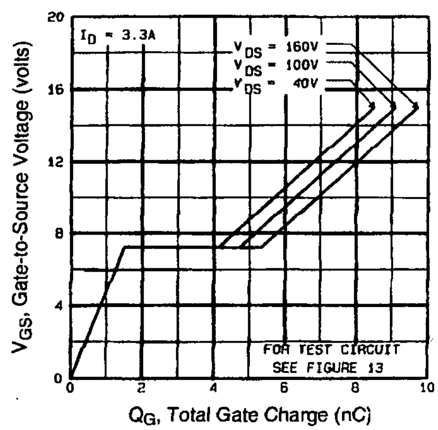


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

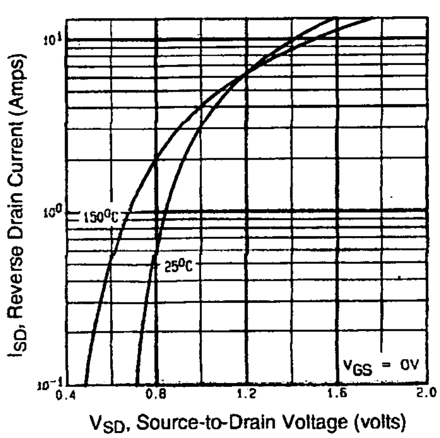


Fig 7. Typical Source-Drain Diode Forward Voltage

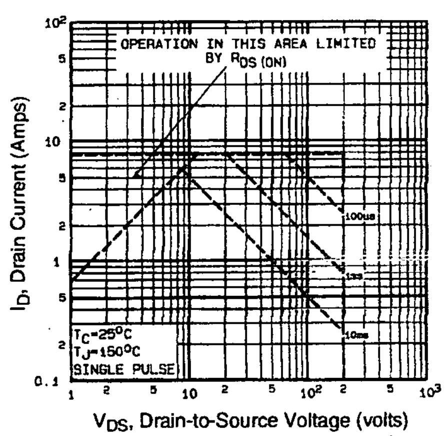


Fig 8. Maximum Safe Operating Area

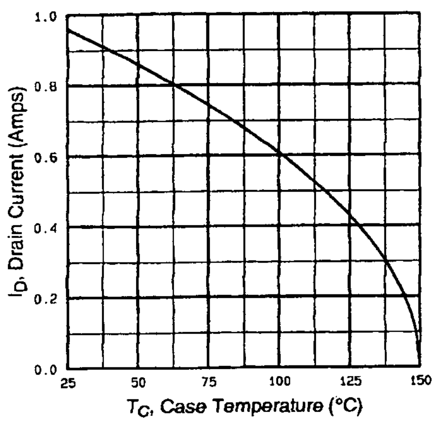


Fig 9. Maximum Drain Current Vs. Case Temperature

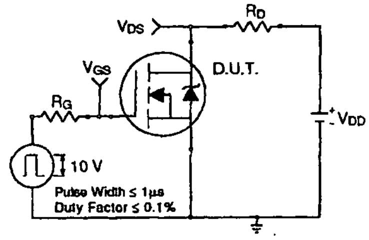


Fig 10a. Switching Time Test Circuit

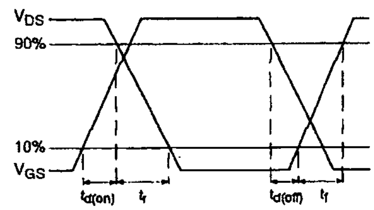


Fig 10b. Switching Time Waveforms

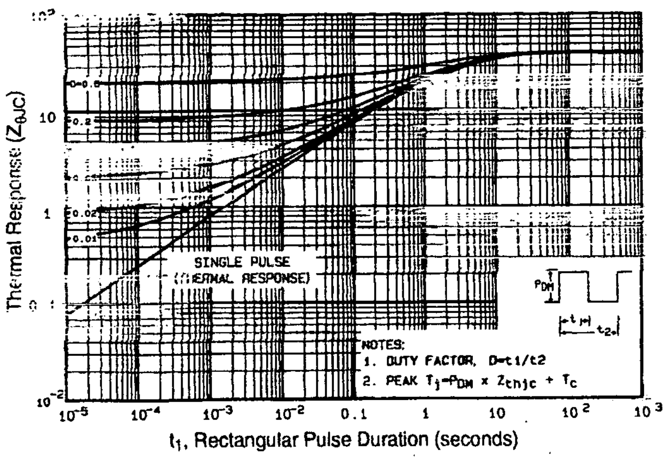


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

DATA SHEETS

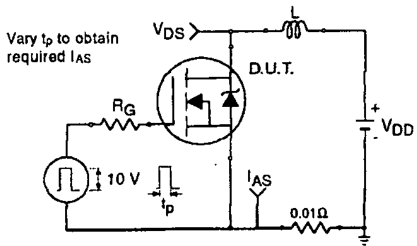


Fig 12a. Unclamped Inductive Test Circuit

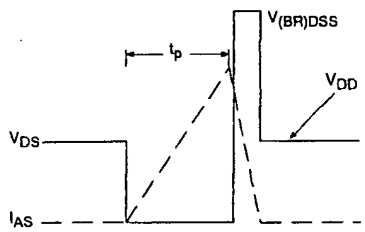


Fig 12b. Unclamped Inductive Waveforms

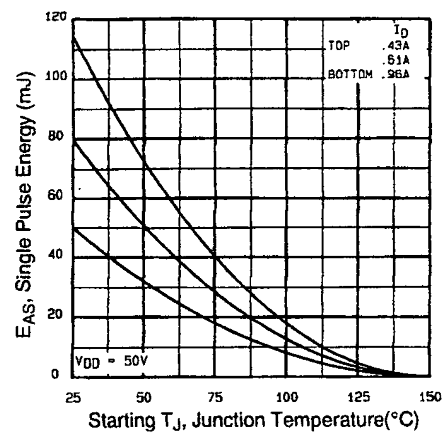


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

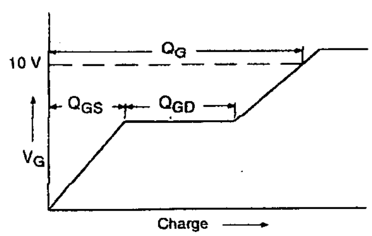


Fig 13a. Basic Gate Charge Waveform

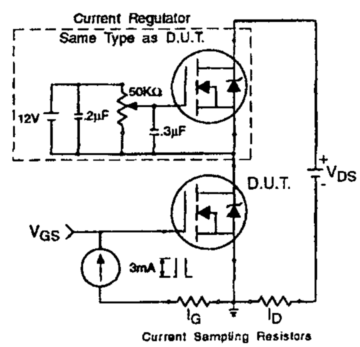


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1505

Appendix B: Package Outline Mechanical Drawing – See page 1508

Appendix C: Part Marking Information – See page 1516

Appendix D: Tape & Reel Information – See page 1522

L5: Entry 3 of 4 File: JPAB Apr 11, 1991

DOCUMENT-IDENTIFIER: JP 03086013 A
TITLE: OVERCURRENT PROTECTIVE CIRCUIT

Abstract Text (2):
CONSTITUTION: Gate of an N-type field effect semiconductor(FET) 1 is connected through a forward diode 3 with the drain of a P-type FET 2, the gate of which is connected through a reverse diode 4 with the drain of the N-type FET 1. Consequently, the N-type FET 1 and the P-type FET 2 function complementarily to interrupt overcurrent and each gate retains the gate voltage at the time of interruption. Each gate retains the gate voltage at the time of interruption for a while even if the voltage between the drains of the FETs 1, 2 drops to 0V, and the N-type FET 1 and the P-type FET 2 are held in interrupted state. By such arrangement, a load circuit can be protected against overcurrent.

Application Date (1):
19890830

10/723939

Refine Search

Your wildcard search against 10000 terms has yielded the results below.

Your result set for the last L# is incomplete.

The probable cause is use of unlimited truncation. Revise your search strategy to use limited truncation.

Search Results -

Terms	Documents
L22 and ((control$ or adjust$) with shift$) same (position$ with (gps$ or satellite$))	0

Database:

US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L23

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Friday, May 26, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; THES=ASSIGNEE; PLUR=YES; OP=OR		
L23	L22 and ((control$ or adjust$) with shift$) same (position$ with (gps$ or satellite$))	0	L23
L22	l19 or l20 or l21	10	L22
	DB=USPT; THES=ASSIGNEE; PLUR=YES; OP=OR		
L21	(5940010 | 6278928 | 5926114)![PN]	3	L21
	DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; THES=ASSIGNEE; PLUR=YES; OP=OR		
L20	('20010034575'| '20020143454'| '6516262') [ABPN1,NRPN,PN,TBAN,WKU]	6	L20
L19	('20010034575'| '20020143454'| '6516262')[URPN]	1	L19

L18	L17 and ((control$ or adjust$) with shift$) and (position$ with (gps$ or satellite$))	3	L18
L17	L16 and (learn$ or "ai" or (artificial$ adj intelligent$) or (neural adj network$)).clm.	358	L17
L16	L15 or l14	54796	L16
L15	(transmission$ shift$) and (gps$ or satellite$) and @pd<=20010330	35114	L15
L14	(transmission$ shift$) and (gps$ or satellite$) and @ad<=20010330	51985	L14
DB=PGPB,USPT; THES=ASSIGNEE; PLUR=YES; OP=OR			
L13	L12 and "gps"	5	L13
L12	(learn$ or "ai" or (artificial$ adj intelligent$) or (neural adj network$)).clm. and L7	54	L12
L11	L10 and "gps"	2	L11
L10	L8 and (learn$ or "ai" or (artificial$ adj intelligent$) or (neural adj network$)).clm.	20	L10
L9	L8 and gps.clm.	5	L9
L8	L7 and (control$ with transmi$ with signal$).clm. and ((electronic$ or electrical$) adj signal$).clm.	2487	L8
L7	(control$ with transmi$ with signal$).clm. and (electronic? or electrical$) adj signal?	5497	L7
DB=PGPB; THES=ASSIGNEE; PLUR=YES; OP=OR			
L6	L5 and (fuel$ same (engine$ with speed$))	1	L6
L5	20020134596	1	L5
DB=USPT; THES=ASSIGNEE; PLUR=YES; OP=OR			
L4	L2 and (fuel$ same (engine$ with speed$))	2	L4
L3	L2 and (fuel$ with cut$)	0	L3
L2	L1 and hybrid$	3	L2
L1	6726593.pn. or 6183389.pn. or 6199650.pn.	3	L1

END OF SEARCH HISTORY

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L1: Entry 1 of 2 File: USPT Mar 29, 2005

US-PAT-NO: 6873171
DOCUMENT-IDENTIFIER: US 6873171 B2

TITLE: Integrated circuit early life failure detection by monitoring changes in current signatures

DATE-ISSUED: March 29, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Reynick; Joseph A.	Whitehall	PA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Agere Systems Inc.	Allentown	PA			02

APPL-NO: 10/777250 [PALM]
DATE FILED: February 12, 2004

PARENT-CASE:
CROSS-REFERENCE TO RELATED APPLICATIONS This Application is a Divisional of prior application Ser. No. 09/558,130 filed on Apr. 25, 2000, now U.S. Pat. No. 6,714,032, to Joseph A. Reynick. The above-listed Application is commonly assigned with the present invention and is incorporated herein by reference as if reproduced herein in its entirety under Rule 1.53(b).

INT-CL-ISSUED: [07] G01 R 31/26

US-CL-ISSUED: 324/765; 324/158.1
US-CL-CURRENT: 324/765; 324/158.1

FIELD-OF-CLASSIFICATION-SEARCH: 324/158.1, 324/765, 365/201, 438/14, 438/17
See application file for complete search history.

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
5889408	March 1999	Miller	
6140832	October 2000	Vu et al.	
6714032	March 2004	Reynick	324/765

☐ 6734028 May 2004 Yang et al. 438/17

OTHER PUBLICATIONS

Thibeault, "A Novel Probabilistic Approach for IC Diagnosis Based on Differential Quiescent Current Signatures", 15th IEEE VLSI Test Symposium, Apr. 27-May 1, 1997, pp. 80-85.
Thibeault et al. "Diagnosis Method Based on Delta-IDDQ Probabilistic Signatures: Experimental Results"; IEEE International Test Conference, 1998 (Month Unavailable), pp. 1019-1026.
Thibeault, "On the Comparison of Delta-IDDQ and IDDQ Testing," VLSI Test Symposium, 17th IEEE Proceedings, Apr. 25-29, 1999, pp. 143-150.
Thibeault, "Improving Delta-IDDQ-Based Test Methods", IEEE International Test Conference Proceedings, Oct. 3-5, 2000; pp.: 207-206.

ART-UNIT: 2829

PRIMARY-EXAMINER: Zarneke; David

ASSISTANT-EXAMINER: Kobert; Russell M.

ABSTRACT:

A method for testing integrated circuits, including measuring a current signature delta value of a device under test and comparing the current signature delta value to a threshold current signature delta value to determine whether the current signature delta value is greater than the threshold current signature delta value. If the current signature delta value exceeds the threshold current signature delta value, the integrated circuit is rejected. Integrated circuits are also rejected if the post-stress current signature value exceeds a maximum current signature value, even though the current signature delta value is less than the threshold current signature delta value. In addition, an apparatus for testing integrated circuits is disclosed.

10 Claims, 4 Drawing figures

Previous Doc Next Doc Go to Doc#

L1: Entry 1 of 2 File: USPT Mar 29, 2005

DOCUMENT-IDENTIFIER: US 6873171 B2
TITLE: Integrated circuit early life failure detection by monitoring changes in current signatures

Detailed Description Text (7):
Threshold current signatures may be formulated for the chosen set of test vectors through process simulation tools, rather than from actual measurements of experimental ICs. The IC is first designed and a full transistor level layout is completed. A switch level (FET) simulation program is used to identify the "off" state n-type FETs and "off" state p-type FETs for each I.sub.ddq test vector. In essence, areas off transistors of each type are "lumped," effectively creating one large n-type FET and one large p-type FET. Since p-type FETs tend to be leakier than n-type FETs, it is preferable to keep separate area sums. Reverse bias diode leakage and sub-threshold leakage current values are usually the dominant contributors to transistor leakage. These parameters are largely process dependent and will be supplied for each distinct process. A simulation is then run using the supplied n-type FET and p-type FET sums together with the reverse diode leakage and sub-threshold leakage for the process of interest to generate a threshold current band for each I.sub.ddq vector. Individual threshold current bands are combined to generate a threshold current signature. Production IC data is then taken for each I.sub.ddq vector and the results compared to the appropriate model values. Random out of specification ICs indicate defects in the IC process or the affected device. However, if failures are consistently registered, it is likely the IC process is running out of specification on one or more critical parameters or the simulated leakage model values require revision. Finally, it should be noted that use of the lumped method ignores geometrical effects that can contribute to leakage.

Detailed Description Text (8):
A modification of the "lumped" simulation method is a gate level modeling method. This method models the IC by representing the IC by a series of logical gates, such as "and" gates and "or" gates. A simulator is preferably used to determine appropriate input sensitization values to put the logical gates into a low current state and determine which transistors that are in the off state. The simulator would be given the off state n-type FET and p-type FET area sums for each distinct cell found in a given IC together with the reverse diode leakage and sub-threshold leakage for the process of interest as in the lumped method to determine leakage on a logical cell basis for each Iddq vector. The simulator would multiply the simulated cell leakage of individual cells by the number of cells in the IC of interest to determine I.sub.ddq values for each test vector. Threshold current signatures may then be formulated for the chosen set of test vectors. Production IC data is then taken for each I.sub.ddq vector and the results compared to the appropriate simulated gate level model values.

L18: Entry 3 of 3 File: USPT Feb 4, 2003

DOCUMENT-IDENTIFIER: US 6516262 B2
TITLE: Running control device for a vehicle

Application Filing Date (1):
20010223

Detailed Description Text (6):
On the other hand, the road information obtaining means 2 can be realized by employing a navigation device as means for calculating a distance L to an intersection, to which an own vehicle is approaching, using an own position obtained by GPS or the like and a road map. The road information obtaining means 2 can be constructed with the navigation device 20 utilizing GPS as shown in FIG. 3 and a GPS antenna 21, for example. Namely, a traveling position of the own vehicle is derived utilizing the GPS to discriminate a road on which the own vehicle is traveling and an intersection, to which the own vehicle is approaching by establishing correspondence between the derived traveling position and the road map stored in the navigation device 20, to calculate a distance L to the intersection, to which the own vehicle is approaching is calculated from information, such as shape of the road or so forth stored in the road map. Since the discriminated road and the intersection are stored in the road map with assigning unique numbers, the road number and the intersection number can be output together with the discriminated road and the intersection.

Detailed Description Text (12):
The cruise control means 6 is a control device for driving the own vehicle to travel with maintaining the distance to the preceding vehicle constant, and is constructed as shown in FIG. 5, for example. The cruise control means 6 includes a radar 605 having a target distance (Dr) setting means 607, a relative speed (Vr) detecting means 602, a distance (Dm) detecting means 604, a speed command (Vcmd) setting means 608, a vehicle speed control means 609, an own vehicle speed detecting means 610, a throttle actuator 611, a transmission actuator 612 and a brake actuator 613.

Detailed Description Text (16):
The vehicle speed control means 609 derives a throttle valve open degree command, a shift command and a brake command on the basis of the own vehicle speed Vo, the speed command Vcmd, the distance Dm, the relative speed Vr, the control mode M and the speed command Vcop to control the throttle actuator 611, the transmission actuator 612 and the brake actuator 613.

Detailed Description Text (27):
When Tcmd.gtoreq.Tth, acceleration control mainly using the throttle open degree command and deceleration control mainly using engine braking are performed. At step 406, the throttle open degree command is set. The throttle open degree command is set from a target engine torque and an engine revolution speed by calculating the target engine torque from a current transmission speed ratio and the speed control target torque Tcmd. This utilizes a relationship between the engine revolution speed, the throttle valve open degree and the engine torque.

Detailed Description Text (28):
Next, at step 407, a shifting command is set. When the speed command target torque Tcmd requires deceleration by engine braking, the shifting command is set for performing down-shifting. Then, at step 408, a brake command is set. Here, since it is not required to operate the brake, the brake command is set for releasing the brake.

Detailed Description Text (29):
On the other hand, when Tcmd<Tth, deceleration control is performed mainly using the brake. At step 409, since deceleration is performed by controlling the brake, the throttle open degree is set to fully close. At step 410, a transmission speed ratio of the transmission actuator 612 is set. At step 411, the brake command is set depending upon the speed command target torque Tcmd. Then, on the basis of the throttle open degree command, the throttle actuator 611 is driven. The transmission actuator 612 is driven on the basis of the shift command. The brake actuator 613 is driven on the basis of the brake command. Thus, own vehicle speed is controlled.

CLAIMS:

4. A cruise control system for an automotive vehicle as set forth in claim 1, wherein said traffic signal characteristics obtaining means includes traffic signal characteristics measuring means for measuring characteristics of the traffic signal and traffic signal characteristics learning means for learning a traffic signal characteristics measured by the traffic signal characteristics measuring means.

5. A cruise control system for an automotive vehicle as set forth in claim 4, wherein said traffic signal characteristics learning means learns intersection information from said road information obtaining means with correspondence to the intersection information.

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Your result set for the last L# is incomplete.

The probable cause is use of unlimited truncation. Revise your search strategy to use limited truncation.

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Search Results - Record(s) 1 through 3 of 3 returned.

☐ 1. Document ID: US 20020143454 A1

Using default format because multiple data bases are involved.

L18: Entry 1 of 3 File: PGPB Oct 3, 2002

PGPUB-DOCUMENT-NUMBER: 20020143454
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020143454 A1

TITLE: Method and system for controlling an automatic transmission using a GPS assist having a learn mode

PUBLICATION-DATE: October 3, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Bates, Cary Lee	Rochester	MN	US
Crenshaw, Robert James	Apex	NC	US
Day, Paul Reuben	Rochester	MN	US
Santosuosso, John Matthew	Rochester	MN	US

US-CL-CURRENT: 701/51; 701/65

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 20010034575 A1

L18: Entry 2 of 3 File: PGPB Oct 25, 2001

PGPUB-DOCUMENT-NUMBER: 20010034575
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010034575 A1

TITLE: Running control device for a vehicle

PUBLICATION-DATE: October 25, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Takenaga, Hiroshi	Tokai-mura		JP
Kuragaki, Satoru	Hitachi		JP
Morizane, Hiroto	Hitachi		JP

US-CL-CURRENT: 701/96; 180/170

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D

☐ 3. Document ID: US 6516262 B2

L18: Entry 3 of 3 File: USPT Feb 4, 2003

US-PAT-NO: 6516262
DOCUMENT-IDENTIFIER: US 6516262 B2

TITLE: Running control device for a vehicle

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
L17 and ((control$ or adjust$) with shift$) and (position$ with (gps$ or satellite$))	3

Display Format: [-] Change Format

Previous Page Next Page Go to Doc#

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End of Result Set

Generate Collection Print

L10: Entry 1 of 1 File: USPT Apr 12, 2005

US-PAT-NO: 6878996
DOCUMENT-IDENTIFIER: US 6878996 B2

TITLE: MOS power transistor

DATE-ISSUED: April 12, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rothleitner; Hubert	Villach			AT

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Infineon Technologies AG	Munich			DE	03

APPL-NO: 10/447649 [PALM]
DATE FILED: May 29, 2003

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
DE	102 23 950	May 29, 2002

INT-CL-ISSUED: [07] H01 L 29/76, H01 L 29/94

US-CL-ISSUED: 257/341; 257/357, 257/371
US-CL-CURRENT: 257/341; 257/357, 257/371, 257/E27.062, 257/E27.063, 257/E29.063, 257/E29.256, 257/E29.268

FIELD-OF-CLASSIFICATION-SEARCH: 257/341, 257/357, 257/365, 257/369, 257/371
See application file for complete search history.

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
5581103	December 1996	Mizukami	257/355
6245607	June 2001	Tang et al.	
6489653	December 2002	Watanabe et al.	257/343

☐				
☐	6747318	June 2004	Kapre et al.	257/368

ART-UNIT: 2814

PRIMARY-EXAMINER: Cao; Phat X.

ASSISTANT-EXAMINER: Doan; Theresa T.

ATTY-AGENT-FIRM: Greenberg; Laurence A. Stemer; Werner H. Mayback; Gregory L.

ABSTRACT:

An integrated MOS power transistors, in particular a lateral PMOS power transistor and a lateral n-DMOS power transistor, in which the bulk node is disposed in a manner spatially isolated from the source electrode zone. The particular integration structure of the MOS power transistor avoids a parasitic drain-bulk diode, a parasitic body diode and a substrate diode and thereby achieves an area-saving protection against over-currents in the event of reverse voltage polarity between drain and source.

12 Claims, 11 Drawing figures

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End of Result Set

☐ Generate Collection Print

L12: Entry 1 of 1 File: PGPB Sep 5, 2002

PGPUB-DOCUMENT-NUMBER: 20020121810
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020121810 A1

TITLE: Control device for a vehicle occupant protection device

PUBLICATION-DATE: September 5, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Belau, Horst	Langquaid		DE
Swart, Marten	Obertraubling		DE

APPL-NO: 10/113161 [PALM]
DATE FILED: April 1, 2002

RELATED-US-APPL-DATA:
Application 10/113161 is a continuation-of US application PCT/DE00/03350, filed September 26, 2000, UNKNOWN

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	DOC-ID	APPL-DATE
DE	199 47 096.0	1999DE-199 47 096.0	September 30, 1999
DE	100 02 375.4	2000DE-100 02 375.4	January 20, 2000

INT-CL-PUBLISHED: [07] B60 L 1/00

US-CL-PUBLISHED: 307/10.1
US-CL-CURRENT: 307/10.1

REPRESENTATIVE-FIGURES: 1

ABSTRACT:

A vehicle occupant protection device having a firing cap for activating the vehicle occupant protection device is controlled with a control device. An energy source provides a supply voltage for the firing cap. A switching transistor connects the firing cap to the energy source. A controlled path of the switching transistor, the energy source, and the firing cap are connected in series with respect to one another. An actuation or control circuit is connected upstream of a control terminal of the switching transistor and controls the switching transistor in such a way that a resistance of the controlled path in the switched-on state of the transistor is kept constant, a signal which is present at the control terminal at

that time is evaluated, an energy which is converted in the switching transistor is determined from the signal at the control terminal and, when a predefined energy limiting value is reached, the switching transistor is switched off.

CROSS-REFERENCE TO RELATED APPLICATION:

[0001] This application is a continuation of copending International Application No. PCT/DE00/03350, filed Sep. 26, 2000, which designated the United States.

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L1: Entry 2 of 2 File: USPT Mar 30, 2004

US-PAT-NO: 6714032
DOCUMENT-IDENTIFIER: US 6714032 B1

TITLE: Integrated circuit early life failure detection by monitoring changes in current signatures

DATE-ISSUED: March 30, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Reynick; Joseph A.	Lehigh County	PA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Agere System Inc.	Allentown	PA			02

APPL-NO: 09/558130 [PALM]
DATE FILED: April 25, 2000

INT-CL-ISSUED: [07] G01 R 31/26

US-CL-ISSUED: 324/765; 324/158.1
US-CL-CURRENT: 324/765; 324/158.1

FIELD-OF-CLASSIFICATION-SEARCH: 324/158.1, 324/765, 365/201
See application file for complete search history.

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5519333	May 1996	Righter	324/765
☐	5790565	August 1998	Sakaguchi	371/27.1
☐	5889408	March 1999	Miller	324/765
☐	5917331	June 1999	Persons	324/765
☐	5939894	August 1999	Yamauchi et al.	324/765
☐	5939897	August 1999	Ayers et al.	326/58
	5944847	August 1999	Sanada	714/741

☐				
☐	5963492	October 1999	Hsu	365/201
☐	6140832	October 2000	Vu et al.	324/765

OTHER PUBLICATIONS

Thibeault, "A Novel Probabilistic Approach for IC Diagnosis Based on Differential Quiescent Current Signatures," 15th IEEE VLSI Test Symposium, Apr.27-May 1, 1997, pp. 80-85.*
Thibeault et al, "Diagnosis method based on Delta-Iddq probabilistic signatures: Experimental results," IEEE International Test Conference, 1998 (Month Unavailable), pp. 1019-1026.*
Thibeault, "On the Comparison of Delta-IDDQ and IDDQ Testing," VLSI Test Symposium, 17th IEEE Proceedings, Apr. 25-29, 1999, pp. 143-150.*
Thibeault, "Improving Delta-IDDQ-based test methods," IEEE International Test Conference Proceedings, Oct. 3-5, 2000, pp. 207-206.*
Nguyen, S.V., "High-Density Plasma Chemical Vapor Deposition of Silicon-Based Dielectric Films for Integrated Circuits," IBM Journal of Research & Development, vol. 43, No. 1/2 (1999). (Month Unavailable).

ART-UNIT: 2829

PRIMARY-EXAMINER: Cuneo; Kamand

ASSISTANT-EXAMINER: Kobert; Russell M.

ABSTRACT:

A method for testing integrated circuits, including measuring a current signature delta value of a device under test and comparing the current signature delta value to a threshold current signature delta value to determine whether the current signature delta value is greater than the threshold current signature delta value. If the current signature delta value exceeds the threshold current signature delta value, the integrated circuit is rejected. Integrated circuits are also rejected if the post-stress current signature value exceeds a maximum current signature value, even though the current signature delta value is less than the threshold current signature delta value. In addition, an apparatus for testing integrated circuits is disclosed.

32 Claims, 4 Drawing figures

Previous Doc Next Doc Go to Doc#

L1: Entry 1 of 1 File: USPT Nov 7, 2000

US-PAT-NO: 6142130
DOCUMENT-IDENTIFIER: US 6142130 A

TITLE: Low inductance high energy inductive ignition system

DATE-ISSUED: November 7, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ward; Michael A. V.	Lexington	MA	02476	

APPL-NO: 09/284810 [PALM]
DATE FILED: April 21, 1999

PARENT-CASE:
This application claims priority under 35 U.S.C. 119(e) of provisional applications Ser. No. 60/008,599, filed Dec. 13, 1995; Ser. No. 60/011,739, filed Feb. 15, 1996; and Ser. No. 60/029,145, filed Oct. 21, 1996.

PCT-DATA:

APPL-NO	DATE-FILED	PUB-NO	PUB-DATE	371-DATE
PCT/US96/19898	December 12, 1996	WO97/21920	Jun 19, 1997	Apr 21, 1999

INT-CL-ISSUED: [07] F02 P 3/05

US-CL-ISSUED: 123/606; 123/620, 123/634, 361/263
US-CL-CURRENT: 123/606; 123/620, 123/634, 361/263

FIELD-OF-CLASSIFICATION-SEARCH: 123/598, 123/605, 123/606, 123/609, 123/620, 123/634, 123/637, 123/643, 123/644, 361/263
See application file for complete search history.

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4522185	June 1985	Nguyen	123/637
☐	5056497	October 1991	Akagi et al.	123/609

☐	5193514	March 1993	Kobayashi et al.	123/634
☐	5315982	May 1994	Ward et al.	123/634
☐	5558071	September 1996	Ward et al.	123/598

ART-UNIT: 377

PRIMARY-EXAMINER: Dolinar; Andrew M.

ATTY-AGENT-FIRM: Perkins, Smith&Cohen, LLP Cohen; Jerry

ABSTRACT:

A high power, high energy inductive ignition system with a parallel array of multiple ignition coils Ti (2a, 2b) and associated 600 volt unclamped IGBT power switches Si (8a, 8b), for use with an automotive 12 volt storage battery (1), the system having an internal voltage source (12) to generate a voltage Vc approximately three times the peal primary coil current with coils Ti of low primary inductance of about 0,5 millihenry and of open E-type core structure for spark energy in the range of 120 to 250 mj, the system using a lossless snubber and variable control inductor (6) to provide very high circuit and component efficiency and high coil energy density, in mj/gm, three times that of conventional inductive ignition systems, and high output voltage of 40 kilovolts with fast rise time of 10 microseconds.

82 Claims, 17 Drawing figures

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Search Results - Record(s) 1 through 4 of 4 returned.

☐ 1. Document ID: US 6714032 B1

Using default format because multiple data bases are involved.

L5: Entry 1 of 4 File: USPT Mar 30, 2004

US-PAT-NO: 6714032
DOCUMENT-IDENTIFIER: US 6714032 B1

TITLE: Integrated circuit early life failure detection by monitoring changes in current signatures

DATE-ISSUED: March 30, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Reynick; Joseph A.	Lehigh County	PA		

US-CL-CURRENT: 324/765; 324/158.1

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 2. Document ID: US 3631264 A

L5: Entry 2 of 4 File: USPT Dec 28, 1971

US-PAT-NO: 3631264
DOCUMENT-IDENTIFIER: US 3631264 A

TITLE: INTRINSICALLY SAFE ELECTRICAL BARRIER SYSTEM AND IMPROVEMENTS THEREIN

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 3. Document ID: JP 03086013 A

L5: Entry 3 of 4 File: JPAB Apr 11, 1991

PUB-NO: JP403086013A
DOCUMENT-IDENTIFIER: JP 03086013 A
TITLE: OVERCURRENT PROTECTIVE CIRCUIT

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

A 4. Document ID: JP 3508965 B2, JP 09214311 A

L5: Entry 4 of 4 File: DWPI Mar 22, 2004

DERWENT-ACC-NO: 1997-464010
DERWENT-WEEK: 200421

TITLE: Switching element driving circuit for switch mode power supply, inverter circuit, motor - has diode connected between drain of FET and gate of switching element through which driving power supply is applied to switching element

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
L4 and @ad<=20021126	4

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L5: Entry 1 of 4 File: USPT Mar 30, 2004

DOCUMENT-IDENTIFIER: US 6714032 B1
TITLE: Integrated circuit early life failure detection by monitoring changes in current signatures

Application Filing Date (1):
20000425

Detailed Description Text (7):
Threshold current signatures may be formulated for the chosen set of test vectors through process simulation tools, rather than from actual measurements of experimental ICs. The IC is first designed and a full transistor level layout is completed. A switch level (FET) simulation program is used to identify the "off" state n-type FETs and "off" state p-type FETs for each I.sub.ddq test vector. In essence, areas off transistors of each type are "lumped," effectively creating one large n-type FET and one large p-type FET. Since p-type FETs tend to be leakier than n-type FETs, it is preferable to keep separate area sums. Reverse bias diode leakage and sub-threshold leakage current values are usually the dominant contributors to transistor leakage. These parameters are largely process dependent and will be supplied for each distinct process. A simulation is then run using the supplied n-type FET and p-type FET sums together with the reverse diode leakage and sub-threshold leakage for the process of interest to generate a threshold current band for each I.sub.ddq vector. Individual threshold current bands are combined to generate a threshold current signature. Production IC data is then taken for each I.sub.ddq vector and the results compared to the appropriate model values. Random out of specification ICs indicate defects in the IC process or the affected device. However, if failures are consistently registered, it is likely the IC process is running out of specification on one or more critical parameters or the simulated leakage model values require revision. Finally, it should be noted that use of the lumped method ignores geometrical effects that can contribute to leakage.

Detailed Description Text (8):
A modification of the "lumped" simulation method is a gate level modeling method. This method models the IC by representing the IC by a series of logical gates, such as "and" gates and "or" gates. A simulator is preferably used to determine appropriate input sensitization values to put the logical gates into a low current state and determine which transistors that are in the off state. The simulator would be given the off state n-type FET and p-type FET area sums for each distinct cell found in a given IC together with the reverse diode leakage and sub-threshold leakage for the process of interest as in the lumped method to determine leakage on a logical cell basis for each Iddq vector. The simulator would multiply the simulated cell leakage of individual cells by the number of cells in the IC of interest to determine I.sub.ddq values for each test vector. Threshold current signatures may then be formulated for the chosen set of test vectors. Production IC data is then taken for each I.sub.ddq vector and the results compared to the appropriate simulated gate level model values.

L5: Entry 2 of 4 File: USPT Dec 28, 1971

DOCUMENT-IDENTIFIER: US 3631264 A
TITLE: INTRINSICALLY SAFE ELECTRICAL BARRIER SYSTEM AND IMPROVEMENTS THEREIN

Application Filing Date (1):
19700211

Detailed Description Text (29):
The barriers illustrated are positive barriers. That is to say, they preform their functions for terminals 1 positive with respect to ground. (They would be short circuits for terminals 1 negative with respect to ground, which is therefore a fail-safe condition.) The negative counterparts exist. For example, reverse all the diodes of FIGS. 1, 2 and 3, replace the N-channel FET's of FIG. 2 with P-channel FET's, and replace the NPN-transistors of FIG. 2 with PNP's. The barrier array will then perform its functions for terminals 1 negative with respect to ground (and fail-safe by shorting the terminals 1 to ground if they turn positive).